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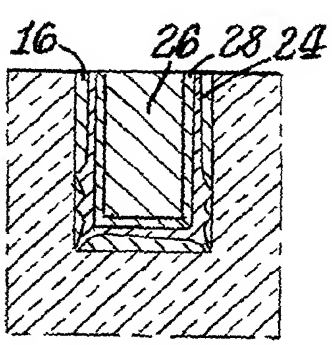
(54) Title: BARRIER ENHANCEMENT PROCESS FOR COPPER INTERCONNECTS




(57) Abstract: A damascene process for introducing copper into metallization layers in microelectronic structures includes a step of forming an enhancement layer of a metal alloy, such as a copper alloy or Co-W-P, over the barrier layer, using PVD, CVD or electrochemical deposition prior to electrochemically depositing copper metallization. The enhancement layer has a thickness from 10Å to 100Å and conformally covers the discontinuities, seams and grain boundary defects in the barrier layer. The enhancement layer provides a conductive surface onto which a metal layer, such as copper metallization, may be applied with electrochemical deposition. Alternatively, a seed layer may be deposited over the enhancement layer prior to copper metallization.

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# Barrier Enhancement Process for Copper Interconnects

This invention relates to an electrochemical deposition process for depositing a thin film enhancement layer onto an existing ultra thin barrier layer to repair defects and enhance the barrier properties of the barrier layer. The deposited thin film enhancement layer serves as a barrier layer and as a seed layer for subsequent copper plating processes.

## Cross-Reference to Related Application

This application claims priority from U.S. Provisional Application Serial No. 60/298,138, filed July 25, 2001.

## Background of the Invention

Metallization patterns are needed to interconnect numerous devices to form integrated circuits. For high performance ultra large scale integration (ULSI) chips, six or more metallization layers are commonly used. The number of layers is expected to increase as the industry works to decrease device dimensions and pack more devices onto integrated circuit chips.

Integrated circuit chip performance is limited by the signal propagation delay of the interconnections, also known as the "RC" delay. In order to improve circuit speed, it is important to reduce both the R (the resistance) and the C (the capacitance) associated with the interconnections. Recently, copper metallization has been introduced to replace aluminum metallization in integrated circuit fabrication because copper has both a lower resistivity and a higher current carrying capacity than aluminum.

Copper metallization requires different processing than aluminum metallization. Instead of metal deposition followed by patterning as used in forming aluminum interconnects, copper interconnects usually are formed using a damascene process. In a damascene process, the conductor pattern is first etched into the dielectric material. Then, the etched patterns are filled with copper. Excess copper

then is removed from over the field using a chemical mechanical polishing ("CMP") step. A via-hole is used to connect different metallization layers formed in the integrated circuit chip. When the conductor line pattern and via-hole pattern are filled and polished separately, the process is generally referred to as a "single damascene" process. When both the conductor line and the via-hole pattern are filled at the same time, the process is generally referred to as a "dual damascene" process.

In the known damascene process, a barrier layer and then a seed layer are deposited over the patterned dielectric layer surface before copper is introduced. The barrier layer is needed to prevent the copper from diffusing into the device region. When in contact with silicon, copper spoils the silicon device operation. Usually, thin refractory metals or metal nitrides are selected for the barrier layer. Representative barrier layer materials include tantalum, tantalum nitride, tungsten, tungsten nitride, titanium and titanium nitride. The seed layer is needed to provide the conductivity for the electrochemical deposition reaction and to provide nucleation sites for the subsequent copper electroplating. Usually, a thin copper layer is deposited over the barrier layer to serve as the seed layer.

One of the most important requirements for the damascene process for copper is to have the deposited copper perfectly fill the small geometries of etched lines or trenches and holes with high aspect ratios (calculated as depth divided by width). Electroplating processes are generally used to deposit copper because such processes have better gap filling capability as compared to physical vapor deposition ("PVD") or chemical vapor deposition ("CVD"). Because electrochemical copper deposition processes can deposit more copper inside small trenches than outside the trenches, they are frequently called "super-filling."

The PVD techniques include, for example, various evaporation and sputtering techniques, such as DC and/or RF plasma sputtering, bias sputtering, magnetron sputtering, ion plating, or ionized metal plasma sputtering. PVD processes generally

produce non-conformal deposition due to their anisotropic and directional nature. The CVD techniques include, for example, thermal CVD, plasma enhanced CVD, low pressure CVD, high pressure CVD, and metal-organo CVD. CVD processes most frequently produce conformal deposition with substantially uniform thickness over the entire surface, including over the field and the bottom and sidewall surfaces of the openings.

Currently, the barrier and seed layers are deposited primarily by PVD processes, such as sputtering and ionized sputtering. Frequently, the barrier and seed layers are deposited sequentially in two different vacuum chambers without breaking vacuum to avoid surface contamination. The critical factor in such deposition processes is the film thickness inside the etched patterns, particularly on the sidewall and bottom of etched lines or trenches and via holes. The PVD processes commonly form thinner film layers in these etched patterns than over the flat field region of the dielectric material. The step coverage of these layers has been problematic. The films must be continuous and defect free. A void or defect in the barrier layer will compromise the integrity of the device. A void or defect in the seed layer will lead to a void or defect in the plated copper film.

To improve step coverage, CVD processes have been tried for depositing the barrier and seed layers. The CVD processes have not yielded better results than the PVD processes, and CVD processes are more expensive. Copper seed layers deposited by CVD processes usually have poor adhesion, higher impurities and poor crystal orientation, leading to problems when additional copper is electrochemically deposited over such seed layers. Sometimes PVD is used in conjunction with CVD, such that a separate copper seed layer is deposited by PVD processing over a copper seed layer deposited by CVD, further adding to the expense for CVD processing. Accordingly, PVD processing for barrier and seed layers for copper interconnects has remained preferred despite noted difficulties with step coverage.

Improvements to PVD deposition technology may not suffice to solve problems with film coverage for the barrier layers and seed layers deposited by PVD. As device dimensions continue to decrease, in the future the barrier film layer on the trench sidewall will need to be less than 10 nanometers. Combined technologies may be required to meet the more rigorous requirements.

U.S. Patent No. 6,136,707 teaches a method of combining a first copper seed layer formed by CVD with a second copper seed layer formed by PVD. U.S. Patent No. 6,197,181 discloses a method of combining a first copper seed layer electrolytically deposited from an alkaline plating solution with a second copper seed layer formed by PVD. Both of these patents thus require additional processing steps to achieve better PVD copper seed layer adhesion. However, the methods disclosed in these patents do not solve the problems caused by either a defective barrier layer or a poor interface between the barrier layer and the copper seed layer.

Accordingly, the industry seeks better methods for electrochemically depositing copper into high aspect ratio holes and trenches.

**Summary of the Invention**

The invention comprises processes and apparatus for applying a metal to a microelectronic workpiece where the microelectronic workpiece includes a surface in which are disposed one or more micro-recessed structures. Most commonly, the microelectronic workpiece is a semiconductor wafer, such as a silicon or gallium arsenide semiconductor wafer. Preferably, the metal is copper applied to form metallization layers in trenches or holes or vias or other structures in the semiconductor wafer using a damascene or dual damascene process.

In the process according to the invention, the steps comprise:

(a) forming a barrier layer on the surface of the microelectronic workpiece, including on the walls of the micro-recessed structures;

(b) forming an enhancement layer over the barrier layer, wherein said enhancement layer is comprised of a metal alloy; and

(c) electroplating a metal onto the enhancement layer so as to fill the micro-recessed structure.

Preferably, the enhancement layer is formed to a thickness of 100 Å or less, most preferably from 10Å to 100Å, using an electrochemical deposition process, such as an electroless or an electroplating process. Alternatively, the enhancement layer may be formed using a CVD or PVD process.

In one embodiment, the enhancement layer is formed from a copper alloy, such as Cu-Al, Cu-Mg and/or Cu-Zn. In another embodiment, the enhancement layer is formed from a binary alloy composition, such as Co-P, or a tertiary alloy composition, such as Co-W-P.

The enhancement layer conformally covers the barrier layer, even where the barrier layer has seams, discontinuities or grain boundary defects. For a silicon semiconductor wafer, the barrier layer may be titanium, titanium nitride, or other known barrier layer materials. The enhancement layer is conductive sufficient to permit deposition of a metal, preferably copper, thereon. Thereafter, excess metal is removed from the field surface, such as by chemical mechanical polishing. The deposited metal remains within the microelectronic structure forming the desired interconnect or metallization layer.

In a further embodiment, the process steps comprise:

(a) forming a barrier layer on the surface of the microelectronic workpiece, including on the walls of the micro-recessed structures;

(b) forming an enhancement layer of a metal alloy over the barrier layer;

(c) forming a seed layer over the enhancement layer; and

(d) electroplating a metal onto the enhancement layer so as to fill the micro-recessed structure.

In this alternate embodiment, the seed layer may comprise a further layer of a metal alloy or may comprise a layer of the metal intended to be deposited in the microelectronic structure. Thus, the seed layer may be a copper alloy, a binary alloy such as Co-P, or a tertiary alloy such as Co-W-P. The seed layer is formed with a thickness preferably from 50 Å to 500 Å.

The damascene processes may be carried out in a manufacturing line including a plurality of apparatus for the manufacture of microelectronic circuits or components, where one or more apparatus of the plurality of apparatus are used to apply interconnect metallization in a damascene process to a surface of a microelectronic workpiece used to form the microelectronic circuits or components. The microelectronic workpiece preferably is a silicon or gallium arsenide semiconductor wafer into which has been formed holes or trenches or vias suited for metallization to form microelectronic circuits or components. In such case, the one or more apparatus comprise:

means for applying a barrier layer to a surface of the microelectronic workpiece using a first deposition process, wherein the barrier layer is generally unsuitable for bulk electrochemical deposition of the interconnect metallization;

means for applying an enhancement layer over the barrier layer using a second deposition process, wherein the enhancement layer formed from an alloy composition that is generally suitable for subsequent electrochemical application of a metal to a predetermined thickness representing a bulk portion of the interconnect metallization; and

means for electrochemical application of a metal over the enhancement layer.

Preferably, the means for applying the enhancement layer is equipment for electrochemical deposition, such as equipment for electroless or electroplating processing. Alternatively, the means for applying the enhancement layer may be equipment for CVD or PVD processing. The means for applying the enhancement

layer is capable of applying the enhancement layer conformally over the barrier layer to a thickness of 100 Å or less, preferably from 10 Å to 100 Å thick. The enhancement layer preferably is formed from a metal alloy, such as a copper alloy like Cu-Al, Cu-Mg and/or Cu-Zn, a binary alloy such as Co-P, or a tertiary alloy such as Co-W-P, or possibly even from mixtures of such alloys.

The means for electrochemical application of a metal over the enhancement layer is capable of applying copper as the metal in the damascene process. Once the copper is introduced into the metallization layers or microelectronic structures, a means is provided for removing a portion of the copper metal from the field surface of the microelectronic workpiece. Preferably, the means for removing a portion of the copper metal comprises chemical mechanical polishing equipment.

The apparatus may include a first chamber for applying the barrier layer and a second chamber for applying the enhancement layer. In addition, the optional additional seed layer and the copper metallization layer may be deposited onto the workpiece while the workpiece is in the second chamber used to apply the enhancement layer. Thus, electrochemical deposition of the enhancement layer, the optional seed layer, and the copper metal may be carried out in a single chamber in the apparatus.

**Description of the Figures**

The invention will be more fully understood by referring to the detailed specification and claims taken in connection with the following drawings.

FIG. 1A is a cross-sectional view illustrating a silicon semiconductor wafer that has been etched to form a dielectric pattern trench;

FIG. 1B is a cross-sectional view illustrating the silicon semiconductor wafer with a trench wherein a thin barrier layer, such as tantalum or tantalum nitride, is shown as deposited uniformly over the surface;

FIG. 2 is a cross-sectional view of a silicon semiconductor wafer with a trench that has been coated with a thin barrier layer, and illustrating surface defects most commonly formed in the thin barrier layer;

FIG. 2A is an enlarged cross-sectional view of the coated silicon semiconductor wafer trench of FIG. 2;

FIG. 3 is a cross-sectional view of the silicon semiconductor wafer with a trench that has been coated first with a thin barrier layer, and then with a barrier enhancement layer according to the invention;

FIG. 4 is a cross-sectional view of the silicon semiconductor wafer of FIG. 3, wherein the trench has been filled with copper using an electrochemical deposition method;

FIG. 5 is a cross-sectional view of the silicon semiconductor wafer of FIG. 4 after the surface has been polished to remove excess copper, leaving a completed damascened conductor pattern;

FIG. 6 is a cross-sectional view of an alternate embodiment wherein the silicon semiconductor wafer has a completed damascened conductor pattern, and wherein a copper seed layer has been deposited over the barrier enhancement layer before the trench was filled with copper; and

FIG. 7 is a graph of the deposition rate of Co-W-P alloy barrier enhancement film over a barrier layer at 75°C in angstroms versus time in minutes.

**Description of the Preferred Embodiments**

Referring first to FIG. 1A, a silicon dielectric material **10**, such as $SiO_2$, comprises a semiconductor wafer shown in enlarged partial cross-sectional view. The dielectric material **10** has a trench **12** formed therein.

The surface of the dielectric material **10** is coated with a thin barrier layer **14**, preferably using a PVD process although a CVD process may also be used. The barrier layer generally may be a thin refractory metal or metal nitride. Representative

barrier layer materials include tantalum, tantalum nitride, tantalum silicon nitride, tungsten, tungsten nitride, tungsten silicon nitride, titanium, titanium nitride and titanium silicon nitride, and other tertiary nitrides.

As shown in FIG. 1A, the barrier layer **14** is formed as a continuous layer or film without discontinuities or surface defects. This is the ideal surface coverage for such a barrier layer. The barrier layer thickness is generally from 100Å to 500Å over the field and flat bottom surfaces within the trench, and depending upon the aspect ratio and opening size of the trench, 100Å or less over the trench sidewall. For very small openings with large depths, the deposited film on the sidewall can be too thin, resulting in discontinuities and surface defects.

Referring next to FIGs. 2 and 2A, the barrier layer **16** formed over the dielectric material **10** is shown to have surface coverage defects within the trench **12.** As illustrated in FIG. 2, the barrier layer **16** has not smoothly covered the trench sidewall and flat bottom surface. Seams **18** are left in the bottom corners where the barrier layer has not covered the dielectric material. Discontinuities **20** are breaks in the coverage along the sidewalls. Grain boundaries **22** represent surface defects that inhibit proper adhesion of a subsequent copper seed layer to be formed over the barrier layer in the known damascene process.

Most of the failures in the barrier layer relate to copper diffusion at the grain boundaries because grain boundary diffusion is much faster than the diffusion through the bulk. It has been proposed to "stuff" the grain boundaries to improve the barrier properties of the barrier layer with grain boundary defects. For example, TiN barrier layers are usually annealed in an oxygen atmosphere to "stuff" the oxygen at the grain boundaries. Another method to reduce the diffusion at the grain boundaries is to add other materials to the original barrier metal to form alloys. The added material usually concentrates at the grain boundaries (also called segregation). Alloy composition can be adjusted to satisfy different requirements. For example, copper

alloys, such as Cu-Sn, Cu-Zn, Cu-Mg or Cu-Al can be used as diffusion barriers for copper. The added metal in the alloy usually concentrates on the grain boundary surface or free surface and prevents the copper atoms from moving. Cu-Sn and Cu-Zn are known to slow the corrosion of Cu in air by preventing oxygen diffusion. Recently, Cu-Al has been studied as a diffusion barrier for copper because Al tends to segregate out at the grain boundaries and at the surface.

One of the most difficult issues in depositing a seed layer over the barrier layer is getting good adhesion between the original barrier layer and the seed layer deposited thereon. Plated copper adheres poorly to the barrier layer surface. That is why the seed enhancement layer described in U.S. Patent 6,197,181 was not directly deposited on the barrier layer, but was deposited onto a PVD deposited copper seed layer. A CVD copper seed layer directly deposited onto the barrier layer also has poor adhesion, and a PVD copper seed layer is often used to improve the adhesion of the CVD copper seed layer.

According to the invention, as shown in FIG. 3, a barrier enhancement layer **24** is deposited conformally over the barrier layer **16,** using either a CVD process, a PVD process or an electrochemical process. An electrochemical process or a CVD process are preferred. An electrochemical deposition process, such as electroless and electroplating processes, are most preferred. The barrier enhancement layer is from 10Å to 100Å thick, and covers the defects, such as the seams **18,** the discontinuities **20**, and the grain boundaries **22** present in the barrier layer **16**. The barrier enhancement layer has good step coverage.

The barrier enhancement layer **24** is intended both to enhance the performance of the diffusion barrier layer and to serve as a seed layer for subsequent copper plating processing. Thus, depositing the barrier enhancement layer can eliminate the need for a separate copper seed layer.

The barrier enhancement layer is formed from a conductive metal that will adhere to the barrier layer and will also permit subsequent copper plating. Preferably, the barrier enhancement layer is formed from a binary or tertiary metal alloy material selected from one of the following: cobalt-phosphorous (Co-P) or cobalt-tungsten-phosphorous (Co-W-P); or is formed from a copper alloy, such as Cu-Al, Cu-Mg, Cu-Zn and/or Cu-Sn, or possibly mixtures of such alloys.

Preferably, the alloy material deposited as the barrier enhancement layer is Co-W-P. Electrochemical deposition processes for Co-W-P are described in detail in U.S. Patent 5,695,810, which description is incorporated herein by reference. Typical deposition temperatures for this alloy range from room temperature to 90°C. However, at 90°C, the loss of aqueous electrolyte by evaporation may be excessive, such that a lower temperature, such as 75°C is preferred. The thickness of the deposited Co-W-P layer can be controlled by controlling the deposition time and temperature for a given deposition chemistry. Co-W-P alloy material deposits over a TiN barrier layer at a rate of about 100Å to 200Å per minute at 75°C in an electrochemical deposition process as graphically illustrated in FIG. 6.

The electrochemical deposition processes are preferred for depositing the barrier enhancement layer. Such processes are compatible with the standard copper plating process and equipment already in use in copper interconnect fabrication. The new electrochemical deposition process for the barrier enhancement layer therefore can readily be integrated with existing plating tools by installing a new process chamber in the existing system. A suitable integrated tool configuration is shown in Figure 12 in U.S. Patent 6,017,437. The integrated tool configuration reduces tooling costs and permits a simple wafer processing flow sequence. After the barrier enhancement layer is deposited, the wafer can be transferred directly to the copper plating module to complete the plating process without leaving the plating tool.

After the barrier enhancement layer **24** is applied over the barrier layer **16**, the etched pattern is filled with electroplated copper as shown in FIG. 4. Thereafter, the field surface is polished, preferably by a chemical mechanical polishing ("CMP") step, to remove the excess copper. A completed damascened conductor pattern after the CMP is completed is shown in FIG. 5.

In an alternate embodiment, two separate layers may be deposited onto the barrier layer. As shown in FIG. 6, the enlarged cross-sectional view of the dielectric wafer material **10** has a trench **12** formed therein. A barrier layer **16** is deposited over flat bottom and sidewall surfaces of the trench, and has grain boundaries, seams and discontinuities therein as noted in the prior embodiment. The barrier enhancement layer **24** is again applied over the barrier layer **16**. Thereafter, a seed layer **28** is formed over the barrier enhancement layer **24**. The seed layer **28** may be formed as an alloy, such as used to form the barrier enhancement layer **24** or may be copper metal. Although the seed layer may be deposited by a CVD, PVD or electrochemical deposition process, the electrochemical deposition processes are preferred. Moreover, it is more economical to deposit the barrier enhancement layer and the seed layer using compatible deposition processes, and preferably in the same tool.

## EXAMPLES

### Example 1

A single barrier enhancement layer was deposited over a TiN barrier layer. The TiN barrier layer was sputtered over a silicon dioxide dielectric material. The TiN barrier layer surface was then cleaned and rinsed. A thin electroless Co-W-P layer was then deposited over the TiN barrier layer. The electrolyte used for deposition consisted of:

| | |
|---|---|
| $CoCl \times 6\ H_2O$ | 30g/l |
| $(NH_4)_2WO_4$ | 10g/l |

| | |
|---|---|
| $Na_3C_6H_5O_7 \times H_2O$ | 80g/l |
| $NaH_2PO_2 \times H_2O$ | 20g/l |
| KOH to pH = 9.5 | |

The deposition temperature was 75°C and deposition time was about one minute. The deposited film (about 100Å) had good diffusion properties and was used successfully as the seed layer for subsequent copper plating.

**Example 2**

A sputtered tantalum barrier layer was applied to the silicon dioxide dielectric substrate. Because direct deposition of Co-W-P onto tantalum is known to have marginal adhesion, a thin layer (about 100Å) of cobalt was sputtered onto the tantalum surface. Then, a layer of Co-W-P was deposited by electroless deposition onto the sputtered Co surface at 75°C for about one minute. The combined film (approximately 200Å) resulted in satisfactory adhesion. Copper was then directly electroplated onto the Co-W-P layer. In this example, the Co layer was the barrier enhancement layer and the Co-W-P was the seed layer for copper plating.

This example illustrates that according to the second embodiment of the invention: (1) two different layers may be used – a barrier enhancement layer and a seed layer; and (2) different deposition techniques were used for depositing the barrier enhancement layer and the seed layer.

The invention has been illustrated by detailed description and examples of the preferred embodiments. Various changes in form and detail will be within the skill of persons skilled in the art. Therefore, the invention must be measured by the claims and not by the description of the examples or the preferred embodiments.

We claim:

1. A process for applying a metal to a microelectronic workpiece, the microelectronic workpiece including a surface in which are disposed one or more micro-recessed structures, the process comprising:

(d) forming a barrier layer on the surface of the microelectronic workpiece, including on the walls of the micro-recessed structures;

(e) forming an enhancement layer over the barrier layer, wherein said enhancement layer is comprised of a metal alloy; and

(f) electroplating a metal onto the enhancement layer so as to fill the micro-recessed structure.

2. The process of claim 1, wherein the enhancement layer is formed using an electrochemical deposition process.

3. The process of claim 2, wherein the electrochemical deposition process is selected from the group consisting of electroless and electroplating processes.

4. The process of claim 1, wherein the enhancement layer is formed using a CVD process.

5. The process of claim 1, wherein the enhancement layer is formed using a PVD process.

6. The process of claim 1, wherein the enhancement layer is formed with a thickness of 100 Å or less.

7. The process of claim 1, wherein the enhancement layer is formed with a thickness in the range of from 10Å to 100Å thick.

8. The process of claim 1, wherein the barrier layer so formed has seams, discontinuities or grain boundary defects, and wherein the enhancement layer conformally covers the barrier layer.

9. The process of claim 1, wherein the enhancement layer is formed from a copper alloy.

10. The process of claim 9, wherein the copper alloy is selected from the group consisting of: Cu-Al, Cu-Mg, Cu-Zn, Cu-Sn, and mixtures of such alloys.

11. The process of claim 1, wherein the enhancement layer is formed from a binary alloy composition.

12. The process of claim 11, wherein the alloy is Co-P.

13. The process of claim 1, wherein the enhancement layer is formed from a tertiary alloy composition.

14. The process of claim 13, wherein the alloy is Co-W-P.

15. The process of claim 1, wherein the metal electroplated onto the enhancement layer is copper.

16. The process of claim 1, further comprising:

(d) removing a portion of the metal from the surface of the microelectronic workpiece.

17. The process of claim 16, wherein the removing is by chemical mechanical polishing.

18. The process of claim 1, wherein the microelectronic workpiece is a silicon or gallium arsenide semiconductor wafer.

19. A metallization layer formed in a microelectronic workpiece according to the process of claim 1.

20. A process for applying a metal to a microelectronic workpiece, the microelectronic workpiece including a surface in which are disposed one or more micro-recessed structures, the process comprising:

(a) forming a barrier layer on the surface of the microelectronic workpiece, including on the walls of the micro-recessed structures;

(b) forming an enhancement layer of a metal alloy over the barrier layer;

(c) forming a seed layer over the enhancement layer; and

(d) electroplating a metal onto the enhancement layer so as to fill the micro-recessed structure.

21. The process of claim 20, wherein the enhancement layer is formed using an electrochemical deposition process.

22. The process of claim 21, wherein the electrochemical deposition process is selected from the group consisting of electroless and electroplating processes.

23. The process of claim 20, wherein the enhancement layer is formed using a CVD process.

24. The process of claim 20, wherein the enhancement layer is formed using a PVD process.

25. The process of claim 20, wherein the enhancement layer is formed with a thickness of 100 Å or less.

26. The process of claim 20, wherein the enhancement layer is formed with a thickness in the range of from 10Å to 100Å thick.

27. The process of claim 20, wherein the barrier layer so formed has seams, discontinuities or grain boundary defects, and wherein the enhancement layer conformally covers the barrier layer.

28. The process of claim 20, wherein the enhancement layer is formed from a copper alloy.

29. The process of claim 28, wherein the copper alloy is selected from the group consisting of: Cu-Al, Cu-Mg, Cu-Zn, Cu-Sn, and mixtures of such alloys.

30. The process of claim 20, wherein the enhancement layer is formed from a binary alloy composition.

31. The process of claim 30, wherein the alloy is Co-P.

32. The process of claim 20, wherein the enhancement layer is formed from a tertiary alloy composition.

33. The process of claim 32, wherein the alloy is Co-W-P.

34. The process of claim 20, wherein the metal electroplated onto the enhancement layer is copper.

35. The process of claim 20, further comprising:

(e) removing a portion of the metal from the surface of the microelectronic workpiece.

36. The process of claim 35, wherein the removing is by chemical mechanical polishing.

37. The process of claim 20, wherein the microelectronic workpiece is a silicon or gallium arsenide semiconductor wafer.

38. A metallization layer formed in a microelectronic workpiece according to the process of claim 20.

39. In a manufacturing line including a plurality of apparatus for the manufacture of microelectronic circuits or components, one or more apparatus of the plurality of apparatus being used for applying interconnect metallization in a damascene process to a surface of a microelectronic workpiece used to form the microelectronic circuits or components, the one or more apparatus comprising:

means for applying a barrier layer to a surface of the microelectronic workpiece using a first deposition process, wherein the barrier layer is generally unsuitable for bulk electrochemical deposition of the interconnect metallization;

means for applying an enhancement layer over the barrier layer using a second deposition process, wherein the enhancement layer formed from an alloy composition that is generally suitable for subsequent electrochemical application of a metal to a predetermined thickness representing a bulk portion of the interconnect metallization; and

means for electrochemical application of a metal over the enhancement layer.

40. The manufacturing line of claim 39, wherein the means for applying the enhancement layer is equipment for electrochemical deposition.

41. The manufacturing line of claim 40, wherein the means for applying the enchancement layer performs an electrochemical deposition process selected from the group consisting of electroless and electroplating processes.

42. The manufacturing line of claim 39, wherein the means for applying the enhancement layer is equipment for CVD processing.

43. The manufacturing line of claim 39, wherein the means for applying the enhancement layer is equipment for PVD processing.

44. The manufacturing line of claim 39, wherein the means for applying the enhancement layer is capable of applying the enhancement layer conformally over the barrier layer to a thickness of 100 Å or less.

45. The manufacturing line of claim 39, wherein the enhancement layer is formed from a metal alloy selected from the group consisting of: Cu-Al, Cu-Mg, Cu-Zn, Cu-Sn, Co-P, and Co-W-P, and mixtures thereof.

46. The manufacturing line of claim 39, the means for electrochemical application of a metal over the enhancement layer is capable of applying copper as the metal.

47. The manufacturing line of claim 39, further comprising:

means for removing a portion of the metal from the surface of the microelectronic workpiece.

48. The manufacturing line of claim 47, wherein the means for removing a portion of the metal comprises chemical mechanical polishing equipment.

49. The manufacturing line of claim 39, wherein the microelectronic workpiece is a silicon or gallium arsenide semiconductor wafer.

50. An apparatus for applying interconnect metallization in a damascene process to a surface of a microelectronic workpiece used to form microelectronic circuits or components, comprising:

means for applying a barrier layer to a surface of the microelectronic workpiece using a first deposition process, wherein the barrier layer is generally unsuitable for bulk electrochemical deposition of the interconnect metallization;

means for applying an enhancement layer over the barrier layer using a second deposition process, wherein the enhancement layer formed from an alloy composition that is generally suitable for subsequent electrochemical application of a metal to a predetermined thickness representing a bulk portion of the interconnect metallization; and

means for electrochemical application of a metal over the enhancement layer.

51. The apparatus of claim 50, wherein the means for applying the enhancement layer is equipment for electrochemical deposition.

52. The apparatus of claim 51, wherein the means for applying the enchancement layer performs an electrochemical deposition process selected from the group consisting of electroless and electroplating processes.

53. The apparatus of claim 51, wherein the electrochemical deposition equipment comprises a chamber, one or more electrodes, one or more cathodes and a processing fluid to couple the one or more electrodes and the one or more cathodes to the microelectronic workpiece.

54. The apparatus of claim 53, wherein the processing fluid is an electrolyte for electroplating copper or a metal alloy selected from the group consisting of: Cu-Al, Cu-Mg, Cu-Zn, Cu-Sn, Co-P, and Co-W-P, and mixtures.

55. The apparatus of claim 50, wherein the means for applying the enhancement layer is capable of applying the enhancement layer conformally over the barrier layer to a thickness of 100 Å or less.

56. The apparatus of claim 50, wherein the enhancement layer is formed from a metal alloy selected from the group consisting of: Cu-Al, Cu-Mg, Cu-Zn, Cu-Sn, Co-P, and Co-W-P.

57. The apparatus of claim 50, the means for electrochemical application of a metal over the enhancement layer is capable of applying copper as the metal.

58. The apparatus of claim 50, wherein the means for applying the barrier layer is within a first chamber and the means for applying the enhancement layer is within a second chamber of the apparatus.

59. The apparatus of claim 50, wherein the means for applying the enhancement layer is within a first chamber and the means for applying the metal over the enhancement layer is within a second chamber of the apparatus.

60. The apparatus of claim 50, wherein the means for applying the enhancement layer is within a first chamber and the means for applying a metal over the enhancement layer comprises the same means within the first chamber of the apparatus.

61. The apparatus of claim 50, wherein the microelectronic workpiece is a silicon or gallium arsenide semiconductor wafer.

Fig. 1A (Prior Art)

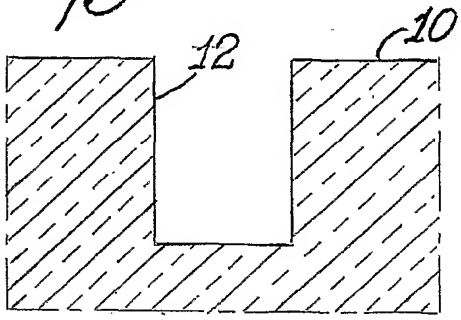



Fig. 1B (Prior Art)

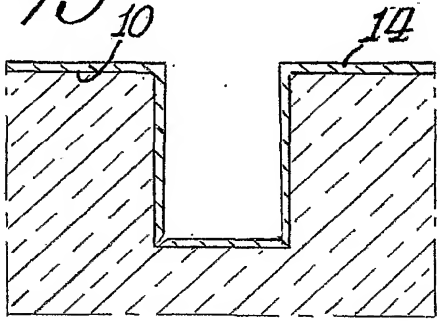



Fig. 2.

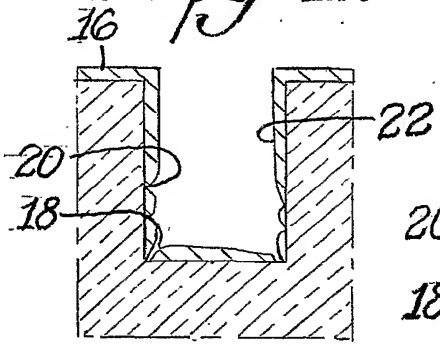



Fig. 2A.

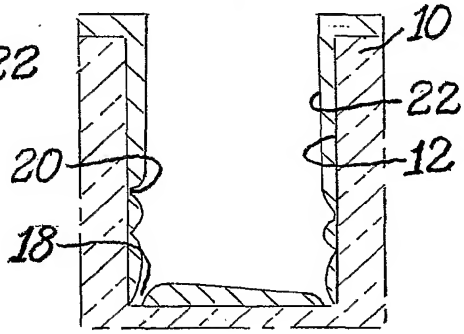



Fig. 3.

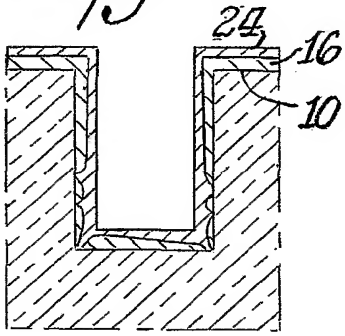



Fig. 4.

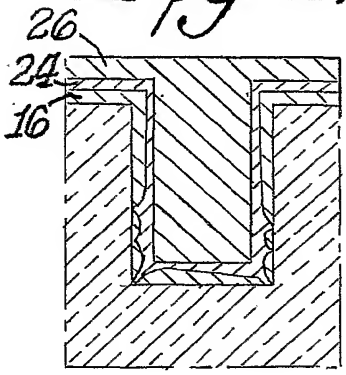



Fig. 5.

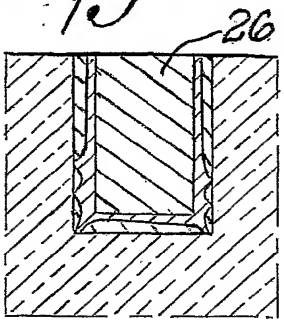
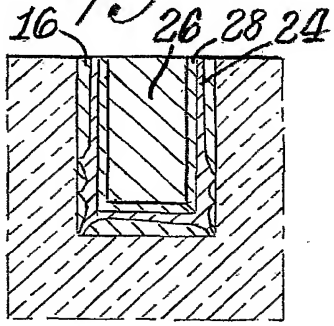



Fig. 6.



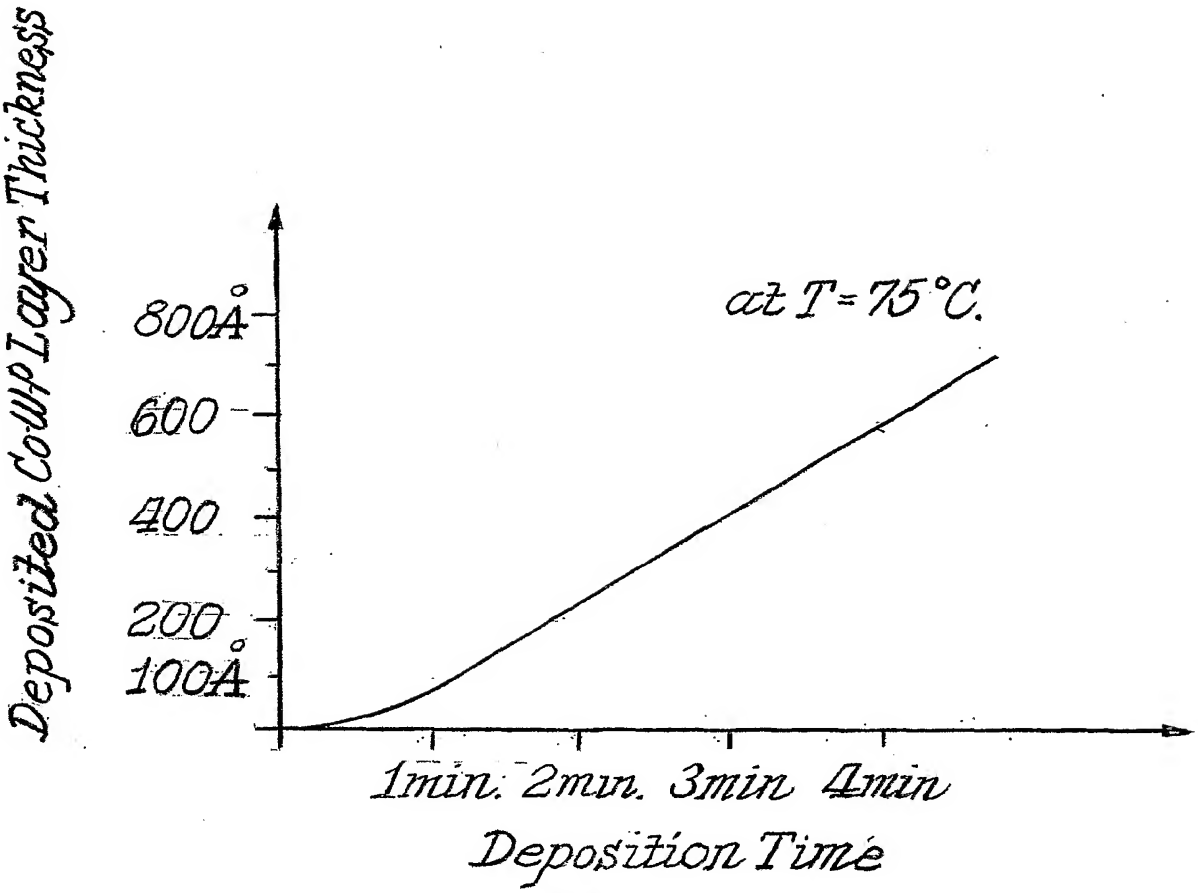

Deposited Co/Ir Layer Thickness
800Å
600
400
200
100Å
at T = 75°C.
1min. 2min. 3min 4min
Deposition Time

Fig. 7.